Abstract—Pulse loads, like solid state pulse modulators, generate short pulses with a high peak power that exceeds the average power by 100 to 1000 times depending on the pulse repetition rate. There, the peak power usually is drawn from an energy buffer such as a capacitor bank. The pulse discharges the energy buffer and it is fully recharged in the time between the pulses by a power supply, which is usually connected to the mains.

Due to the world-wide variation in mains voltages and the desired ability to adapt to the capacitor voltage of the modulator, the power supply has to support a wide input and output voltage range. Additionally, the supply should draw a sinusoidal current from the mains while providing energy to the pulse modulator due to EMI regulations. Therefore, a general control concept for pulse load applications, which guarantees continuous power consumption from the mains and power factor correction (PFC), is described in this paper. Furthermore, measurements of the control principle, which is independent from the converter topology, are presented for a three-phase buck boost rectifier.

Index Terms—Buck Boost Rectifier, Capacitor Charging, Constant Input Power, Pulse Modulator, Power Factor Correction.

I. INTRODUCTION

SOLID state pulsed power systems containing IGBTs are often operated with input voltages between 100V and 6.5kV due to the maximum allowable blocking voltage of the switches. Nevertheless, high output voltages of several kilovolts (e.g. ~100-200kV) can be achieved, for example, by the use of pulse transformers, adder topologies or Marx generator configurations [1],[2].

Generally, the pulse power (e.g. 20MW for the case considered in this paper) is provided from a capacitor bank, whereas the average power (20kW) is supplied by a converter [3] connected to the mains, as shown in Fig. 1. There, the three-phase line-to-line voltage can vary from 177V to 528V to enable world-wide operation.

Additionally, a variation of the capacitor voltage \( v_{C0} \) of the modulator is often desired for adapting the pulse voltage. Therefore, a wide input and output voltage range of the rectifier is needed. These requirements can be fulfilled with a three-phase buck-boost rectifier [4] (cf. Fig. 2), which operates either in the buck or the boost mode, depending on the ratio of the mains voltage to the capacitor bank voltage \( v_{C0} \). In case of the assumed high pulse repetition rate of 500-1000Hz, the capacitor bank has to be recharged before the next pulse is generated, which would demand, especially during load changes, a high dynamic voltage control. There, the voltage should be regulated within ±1% of the reference voltage after 5 pulses for a load step from zero to full load (25kW). This, for example, corresponds to a settling time of 5ms for a pulse repetition frequency of 1000Hz.

To enable unity power factor operation of the three-phase buck-boost rectifier, a constant inductor current \( i_{L0} \) is required [4]-[6]. The pulse load in combination with a conventional high dynamic voltage control, however, would result in periodic peak currents in the buck-boost inductor and also in the input/mains currents \( i_{N,i} \). These current distortions make unity power factor operation of the converter impossible.

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Hence, a control strategy for pulse load applications, which achieves unity power factor as well as accurate regulation of the output voltage, must be applied.

In Section II the operating principle, including the basic structure of the controller [4]-[6], is described. Conventional control of the converter is then explained and its drawbacks, which result in distorted mains, are highlighted in Section III. Following this, the proposed control method is described, which enables approximately constant power consumption with unity power factor. Finally the control approach is validated with measurement results of the input and output current/voltage waveforms, which are presented in Section IV.

II. BUCK BOOST RECTIFIER

As shown in Fig. 2 the input stage of the buck-boost converter consists of six switches $S_1$-$S_6$ with series connected diodes, which are connected to either a common negative or positive voltage terminal. The following boost stage consists of switch $S_6$, diode $D_b$ and the inductance $L_0$. The buck input stage operates as PFC input stage, which produces sinusoidal mains currents.

In case the output voltage $v_{CO}$ is lower than the peak line-to-line mains voltage, only the input stage is used and the converter operates in the buck mode.

For higher output voltages, the boost switch $S_b$ must be activated. The prototype, which has been used for validating the control scheme, is shown in Fig. 3 and the specifications are given in Table I.

In order to limit the current ripple $\Delta i_{L0}$ the converter is operated in continuous conduction mode (CCM) with an average value $i_{L0}$ of the inductor current $i_{L0}$. At high switching frequencies and with a large inductance $L_0$, the ripple current is neglected for simplification. Assuming a constant current $i_{L0}=i_{L0}$, the duty cycles of the buck stage switches directly can be calculated to achieve unity power factor operation, which is described in detail in [4]-[6].

In order to obtain a constant output voltage the duty cycles of the switches must be adapted to the input voltage and the load by a controller. For a symmetrical three-phase supply the control behavior of the three-phase buck boost rectifier can be modeled by a single phase DC-DC converter with constant input voltage [6], as shown in Fig. 4. There, also the proposed and implemented cascaded control structure of the converter with an outer voltage control and an inner current control loop is depicted.

For the control of the output voltage, the voltage $v_{CO}$ is measured and compared to the reference voltage $v_{CO,ref}$. The voltage difference, which is equal to the voltage error $v_e$, is the input of the voltage controller. This controller is implemented as a PI-controller and its output is the reference current $i_{L0,ref}$ for the inner current control loop. The current error $i_e$, which is fed into the current control block, is obtained by subtracting the measured inductance current $i_{L0}$ from the current reference $i_{L0,ref}$. With the error signal $i_e$ the duty cycles $m$ and $d$ of the buck and boost stage are calculated in the current controller. In order to achieve a higher dynamic response an initial current $i_{init}$ can be added to the reference current $i_{L0,ref}$.

III. CONTROL CONCEPT FOR PULSE LOAD APPLICATIONS

The control structure in Fig. 4 is usually designed for continuous loads, where the output voltage is controlled to a constant value. With a constant voltage and a constant load at the output also continuous energy consumption from the mains and sinusoidal mains currents are obtained.

In case of a solid state modulator the power consumption of the load is discontinuous (only a few µs) and has a high peak value (20MW) compared to the average power (20kW). The energy for the pulses is usually provided from capacitor banks (cf. $C_2$ in Fig. 1) [1], [2]. Due to the large peak power the capacitor voltage $v_{CO}$ drops (here: 1%/10V) below its reference values $v_{0,ref}$ during the pulse (cf. Fig. 5). Consequently, the voltage error $v_e$ increases rapidly. Assuming a controller with high dynamic, the “step like”

![Fig. 3](image-url) Photograph of the three-phase buck boost rectifier with unity power factor and a wide input and output range.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>SPECIFICATIONS OF THE CONSIDERED BUCK BOOST RECTIFIER</th>
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<tbody>
<tr>
<td>Input voltage $v_n$</td>
<td>$177V – 528V$</td>
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<tr>
<td>Output voltage $v_{CO}$</td>
<td>$150V – 450V$</td>
</tr>
<tr>
<td>Load current $I_{Load}$</td>
<td>$55A – 167A$</td>
</tr>
<tr>
<td>Average Power $P_{avg}$</td>
<td>$25kW$</td>
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![Fig. 4](image-url) Single phase DC-DC equivalent circuit of the three-phase buck boost converter with cascaded current and voltage control structure.
increase of the error signal results in a rapidly increasing inductor current \( i_{L0} \) for recharging the capacitor bank up to the reference value \( v_{0,\text{ref}} \).

As soon as the reference value is reached the controller must decrease the inductor current down to zero again, since the load current is zero in between two consecutive pulses. This control behavior could be observed after every pulse, what would result in a highly distorted pulsating /discontinuous mains current with a low power factor.

\[ v_{0} = v_{0,\text{ref}} = \text{const.} \]

In case A, which is considered first, the second condition must be always fulfilled, i.e.

\[ i_{L0} = \text{const.} \]

For the pulse modulator with a capacitive storage bank \( C_0 \) the current \( i_{L0} \) respectively the capacitor voltage \( V_{C0} \) has to satisfy equation (3).

\[ \frac{dV_{C0}(t)}{dt} = i_{L0} = \text{const.} \]

Generally, the load current can be expressed as a function of

\[ i_{L0}(t) = \frac{C_0}{1-d} \int v_{C0}(t) \, dt \]

In both cases the first condition only has to be satisfied at the time steps \( n \cdot t_{\text{rep}} \) when the pulses are generated. Therefore,
Fig. 8. Discontinuous inductance current $i_{L0}$ at the beginning of a pulse sequence and after a load change due to the reset of the reference voltage $v_{C0,ref}$ after each pulse (pulse repetition frequency of 1000Hz).

arbitrary complex load impedance $Z_{Load}$:

$$i_{L0} = f(Z_{Load})$$

Integrating (3) for $v_{C0}(t)$ and assuming a constant inductor current $i_{L0}$ results in

$$v_{C0}(t) = \frac{(1-d)}{C_0} \int_0^t I_{L0} dt = v_{C0}(0) + \frac{(1-d)i_{L0}}{C_0} \cdot t$$

Consequently, the capacitor voltage $v_{C0}$ must change linearly in order to achieve a constant current $i_{L0}$ for unity power factor. There also (1) has to be fulfilled.

Thus, a linear increasing reference voltage $v_{C0,ref}$ instead of a constant reference voltage $V_{C0}$ is used for the proposed control method. The slew rate of the reference voltage $v_{C0,ref}$ could be determined with the pulse repetition time $t_{rep}$ and the voltage drop $\Delta v_{C0}$ during the pulse since also (1) must be satisfied.

The initial reference voltage $v_{C0,ref}$ at the end of the pulse is set to the minimum actual capacitor voltage $v_{drop}$ ($v_{C0}(0)$) resulting in

$$v_{C0,ref}(t) = v_{drop} + \frac{\Delta V_{C0}}{t_{rep}} \cdot t = (v_{C0} - \Delta v_{C0}) + \frac{\Delta v_0}{t_{rep}} \cdot t$$

for $t = 0..t_{rep}$.

The waveform of the reference voltage $v_{C0,ref}(t)$ to achieve a constant current $i_{L0}$ and a unity power factor for pulse loads is shown in Fig. 6.

For case B, where the ripple voltage $\Delta V_{C0}$ is large, the inductor current $i_{L0}(t)$ is no longer constant. The power consumption of the converter with capacitive load can be written as

$$P(t) = v_{C0}(t)i_{L0}(t) = C_0 v_{C0}(t) \frac{dv_{C0}(t)}{dt} = \text{const}.$$ (7)

which has to be constant.

Solving (7) leads to the capacitor voltage

$$v_{C0}(t) = \sqrt{\frac{v_0^2 - v_{C0}(0)^2}{t_{rep}} t + v_0^2}$$

which is the reference voltage for large voltage ripples. Based on the capacitor voltage the current in the inductor is given by

Fig. 9. Schematic waveforms of the continuous error voltage $v_e$ and the inductance current $i_{L0}$ at the beginning of a pulse sequence or after a load step (pulse repetition frequency of 1000Hz).

Fig. 10. Spike in the inductance current $i_{L0}$ due to the constant reference voltage $v_{C0,ref}$ during the pulse. Disabling the control during the pulse prevents from a current spike.
\[ i_{L0}(t) = P_{\text{avg}} \left( \frac{v_o^2 - v_{C0}(0)^2}{t_{\text{rep}}} - t + v_0^2 \right)^{-1}. \] (9)

**B. Beginning of pulse sequence and load steps**

The reference voltage in (6) is derived for steady state conditions with a constant load and pulse repetition rate. At the beginning of a pulse sequence, the storage capacitor \( C_0 \) is charged up to \( V_{C0} \) and the buck-boost converter transfers no power to the modulator. After the first pulse is detected, the controller of the buck-boost converter resets the reference voltage \( v_{C0,\text{ref}} \) to \( v_{\text{drop}} \) and ramps \( v_{C0,\text{ref}} \) linearly up to \( V_{C0} \) to recharge the capacitor \( C_0 \) with a constant current \( i_{L0} \). Thereafter, the pulse repetition rate \( t_{\text{rep}} \) must be given by the control of the modulator.

Since the current \( i_{L0} \) in the buck-boost inductor starts from zero and has a limited slew rate, the current \( i_{L0} \) is too small so that the capacitor voltage \( v_{C0}(t) \) can not follow the reference value and it does not reach its nominal value \( V_{C0} \) until the second pulse (cf. Fig. 8). Therefore, the error voltage \( v_e(t) \) is increasing over time and the capacitor voltage \( v_{C0}(t) \) is below the nominal value \( V_{C0} \) at the beginning of the second pulse.

After the second pulse, the voltage reference \( v_{C0,\text{ref}} \) would be reset again to the actual capacitor voltage \( v_{C0}(2t_{\text{rep}}) \) as described for steady state operation. This reset of \( v_{C0,\text{ref}} \) also would lead to a reset of the voltage error \( v_e(2t_{\text{rep}}) = 0 \) and therefore to a sawtooth shaped waveform of \( v_e(t) \) (cf. Fig. 8). Because of the cascaded and highly dynamic control (cf. Fig. 4) the voltage error \( v_e \) would lead to a reference current \( i_{L0,\text{ref}} \), which has a similar shape as the error voltage \( v_e \). Consequently, the waveform of the current \( i_{L0} \) in the buck-boost inductor \( L_0 \) also would be sawtooth-like and the mains currents would be distorted at the beginning of a pulse sequence.

In order to avoid the discontinuities of the error voltage \( v_e \) and the current \( i_{L0} \), the initial value of the reference voltage \( v_{C0,\text{ref}} \) after the pulse has to be reset in such a way, that the error voltage \( v_e \) is continuous. Therefore, the error voltage \( v_e \) before and after the pulse must be equal.

\[ v_e(n \cdot t_{\text{rep}}) = v_e(n \cdot t_{\text{rep}} + t_{\text{pulse}}) \] (7)

This can be achieved by adding the last error voltage \( v_e \) before the pulse to the voltage \( v_{\text{drop}} \). Therefore,

\[ v_{\text{drop}}(n \cdot t_{\text{rep}}) = v_{\text{drop}} + v_e(n \cdot t_{\text{rep}} - t_{\text{pulse}}) \] (8)

Additionally, the slew rate of the voltage reference \( v_{C0,\text{ref}} \) must be adjusted because of the shifted initial voltage \( v_{C0,\text{ref}}(0) \). Therefore, (6) is modified to

\[ v_{\text{drop}}(t) = \left( v_{\text{drop}} + v_e(n \cdot t_{\text{rep}} - t_{\text{pulse}}) \right) + \left( \frac{\Delta v_0 - v_e(n \cdot t_{\text{rep}} - t_{\text{pulse}})}{t_{\text{rep}}} \right) \] (9)

which results in a continuous waveform of \( v_e \) and \( i_{L0} \) (cf. Fig. 9). The described procedure also leads to a continuous error signal \( v_e \) and inductor current after a load step.

**C. Disabling the control during the pulse**

For correct calculation of the reference voltage \( v_{C0,\text{ref}} \), the converter is synchronized with the trigger signal of the modulator. Additionally, the minimum capacitor voltage \( v_{\text{drop}} \) has to be detected after receiving the synchronisation signal. Consequently, the reference voltage \( v_{C0,\text{ref}} \) can not be updated during the pulse until the minimum capacitor voltage \( v_{\text{drop}} \) has been detected and is therefore fixed at \( V_{C0} \) during the pulse as shown in Fig. 10.

Moreover, the voltage error \( v_e \) increases rapidly during the
pulp and the cascaded control would increase the inductor current $i_{L0}$. In order to prevent the controller from increasing the current $i_{L0}$ during the pulse, the voltage controller is disabled, i.e. the current reference $i_{L0,ref}$ and therefore also the current $i_{L0}$ is kept constant, until the voltage reference $v_{C0,ref}$ is updated again.

IV. MEASUREMENT RESULTS

In Fig. 11(a) the reference voltage $v_{C0,ref}$ and the capacitor voltage $v_{C0}$ for a sequence of 20 pulses with a pulse repetition frequency of 720Hz and an average output power of 10kW are shown. At the beginning of the pulse sequence a voltage error, due to the start-up behavior as described before, can be noticed. The corresponding inductance current $i_{L0}$ is depicted in Fig. 11(b). As can be recognized, the current $i_{L0}$ converges to a constant value as soon as the voltage reaches the value $V_0$.

In Fig. 12(a) the inductor current $i_{L0}$ for the same pulse sequence with a pulse repetition frequency of 440Hz and an average output power of 8kW is shown. The corresponding sinusoidal mains current $i_N$ and voltage $v_N$ of one phase are depicted in Fig. 12(b). The measured phase shift is caused by the input filter capacitors and is reduced when the converter operates at the nominal output power of 25kW.

V. SUMMARY

In this paper a control scheme for AC-DC converters with pulsating loads, such as pulse modulators, is explained in detail. This method modulates the reference signal such that continuous power flows from the mains and sinusoidal mains currents are drawn even though the load power consumption is discontinuous. To validate the theoretical concepts, the control, which is basically independent of the converter topology, has been successfully implemented with a three-phase buck-boost converter and measurement results are presented in the paper.

The concept has been derived for pulse modulators with relatively small variations of the DC link voltage. In case of large variations modified reference values, as presented in the paper, for the capacitor voltage must be applied in order to obtain constant power consumption.

REFERENCES